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OFGS File No.	:	P/2850-15
Inventor	:	Yoshiaki Shiota
Title	:	FRAME-RELAY FRAME TRANSMISSION CIRCUIT
Assignee	:	NEC Corporation

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

11 Pages of Specification including Abstract and Claims
11 Numbered Claims Calculated as 11 Claims for Fee Purposes
4 Sheets of Drawing Containing Figures 1 to 5. Formal
1 Declaration and Power of Attorney
X Priority is Claimed under 35 U.S.C. §119:
Convention Date December 26, 1997 for Japanese Appln. S.N. 9-359899
X Certified Priority Application
-- Verified Statement Claiming Small Entity Status under 37 C.F.R. §1.27.
1 Assignment
1 PTO 1449
1 Return-Addressed Post Card

OFGS Check #81986, which includes the fee of $878.00, calculated as follows:

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Number of Independent Claims in Excess of 3, times $78: . .	$ 78.00
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Total Filing Fees or	
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Assignment Recording Fee: $40	$ 40.00
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Respectfully submitted,

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P/2850-15

FRAME-RELAY FRAME TRANSMISSION CIRCUIT

Field of the Invention

The present invention relates to a frame-relay frame transmission circuit using a DMA transmission process, and in particular, to a frame-relay frame transmission circuit for converting a frame-relay frame into an AAL5 (ATM Adaptation Layer type 5) frame.

This application is based on Japanese Patent Application No. Hei 9-359899, the contents of which are incorporated herein by reference.

Background Art

Fig. 1 shows a system for converting a received frame-relay frame into an ATM cell using a device performing a conventional direct memory access (DMA).

A processor 105 performs a process through a processor bus 106 according to an instruction from software. When receiving a frame-relay frame through a channel, a frame receiver 101 in a frame transmission processing device 102 searches for (hunts) a frame buffer. A data FIFO block 103 temporarily stores frame data. A processor bus interface 104 transmits the frame to the searched frame buffer in a memory 107 through the DMA.

A segmentation and reassembly (SAR) device 108 receives frame cell conversion information according to an instruction from the processor, and performs segmentation of the frame into an ATM cell.

The memory 107 is accessed by the processor 105 and the frame transmission processing device 102, and stores the frame cell conversion information 109 for

conversion of the frame into an ATM cell and data 110 of the frame in the frame buffer as shown in Fig. 2.

The operation of the system will be explained. The processor 105 prepares an available frame buffer area in the frame transmission processing device 102. When starting to receive the frame receiver 101, the frame receiver 101 searched for the frame buffer and notifies the processor bus interface 104 of the top address of the frame buffer. The processor bus interface 104 transmits the received frame from the data FIFO block 103 to the memory 107 through the DMA according to the received address. At that time, the transmitted frame is stored in the frame transmission processing device 102. After completion of the transmission, an interrupt notification is sent to the processor 105.

By the software detecting the interrupt, the transmitted frame information is read from the frame transmission processing device 102. A multiprotocol section for the frame-relay frame which is written in the memory 107 is converted into a multiprotocol for ATM Adaptation Layer 5 (AAL5). While an area of an identifier for making a packet (capsuling) and transmitting the multiprotocol is assigned at the top of user data in the frame-relay frame and at the top of the AAL5 frame, the size of the area of the AAL5 frame is greater than the other kinds of protocols. To perform conversion between such protocols, the frame-relay frame is copied into a free area, which is not occupied by the frame data 11, in the memory 107 by the software, and the conversion of the protocols is performed. After completion of the conversion, the processor transfers the frame cell conversion information to the SAR device 108, which converts the frame into the AAL5 frame and produces an ATM cell.

However, there is the problem that the frame transmission processing device

102 may write the frame data from the top of the searched frame buffer. When the area for the multiprotocol of the AAL5 frame is greater than that of the frame-relay frame, the frame-relay frame must be copied into a free area, which is not occupied by the frame data 11, in the memory 107 by software for performing conversion between such protocols, increasing the overhead caused by the conversion process.

This is because the conventional frame transmission processing device 102 is not designed according to concepts in which the frame is lengthened due to the conversion of the transmitted frame data and in which the top of the frame is converted.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a frame-relay frame transmission circuit which can reduce overhead caused by a conversion process.

In order to accomplish the above object, in a frame-relay frame transmission circuit of the present invention, when a received frame-relay frame is written in a memory, the frame is written from an address shifted from the top of a frame buffer. The shift size is determined for each connection.

Further, a frame-relay frame transmission circuit of the present invention for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprises: a processor for determining a shift size for each connection, the shift size by which the frame is to be shifted from the top address of a frame buffer; a frame receiver for receiving the frame through the connection; a memory for storing the received frame in a frame buffer from an address shifted from the top of a frame buffer by the shift size; and a segmentation and reassembling device for reassembling the frame into the ATM cell.

The processor writes a set of data link connection identifiers (DLCI) and the shift size into a connection table, and retrieves the shift size in the connection table using the DLCI as a key. The frame received by the frame receiver is transmitted to the memory through direct memory access.

Furthermore, a method of the present invention for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprises the steps of: determining a shift size for each connection by which the frame is to be shifted from the top address of a frame buffer in a memory; receiving the frame and writing the frame from an address shifted from the top address of the frame buffer by the shift size; and reassembling the frame into an ATM cell.

The method of the present invention further comprises the steps of: writing a set of a data link connection identifier (DLCI) and the shift size into a connection table, and retrieving the shift size in the connection table using the DLCI as a key. The received frame is transmitted to the memory through direct memory access.

The advantage of such a circuit is that, even when a multiprotocol of a frame-relay frame is converted into a multiprotocol of the AAL5 frame, it is unnecessary to copy the frame-relay frame, which was written in a memory through a frame transmission processing device, into another area excluding a memory table for the frame data.

This is because the frame is written from a position which is shifted from the top of a searched frame buffer when the frame transmission processing device 11 writes the frame into the memory.

The second advantage is that the waste of resources due to shifting of all frames can be avoided because a frame which does not need to be shifted is not shifted.

Additional objects and advantages of the present invention will be apparent from the following detailed description of a preferred embodiment thereof, which is best understood with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram showing a conventional frame transmission processing device and peripheral devices.

Fig. 2 is a diagram showing a memory in the conventional device of Fig. 1.

Fig. 3 is a schematic diagram showing a frame transmission processing device and peripheral devices of the present invention.

Fig. 4 is a diagram showing a memory in the device of Fig. 3.

Fig. 5 is a diagram showing a frame which is written from a position shifted from the top of a frame buffer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to figures, the best mode of a frame-relay frame transmission circuit according to an embodiment of the present invention will be explained.

Fig. 3 is a schematic diagram showing a system of the present invention, Fig. 4 shows a memory 16 in detail, and Fig. 5 shows an example of a received frame which is shifted and written from the top of a searched (hunted) frame buffer.

According to an instruction from a software, a processor 14 writes a set of a data link connection identifier (DLCI) and shift information for each reception channel to a memory table A18 which is a connection table. The DLCI is a connection identifier for frame-relay frame, and the shift information indicates how many bytes the

received frame is to be shifted by from the top of the frame buffer. The size of the whole frame buffer and the start address are indicated to a frame transmission processing device 11.

When receiving the top portion of the frame-relay frame from the channel, a frame receiver 10 in the frame transmission processing device 11 performs retrieval in the memory table A18 using the DLCI at the top portion as a key, and obtains the number of the bytes of the shift. The frame receiver 10 searches for (hunts) a frame buffer 21 and instructs a processor bus interface 13 to transmit the frame. An address indicated in the instruction is a shifted top address 22 of the frame buffer which was shifted by a given number of bytes.

According to the indicated top address, the processor bus interface 13 receives the frame from a data FIFO block 12 and transmits it to a memory 16 through a DMA process.

The transmitted frame information is stored in the frame transmission processing device 11. After the transmission is completed, the processor 14 transmits an interrupt notification to the processor 14. Through the software detecting the interrupt, the transmitted frame information is read from the frame transmission processing device 11. A multiprotocol of the frame-relay frame written in the memory 107 is converted into an AAL5 multiprotocol. After conversion, the processor transfers frame cell conversion information in the memory table 19 to a SAR device 17, which converts (reassembles) the frame into the AAL5 frame and produces an ATM cell.

This invention may be embodied in other forms or carried out in other ways without departing from the spirit thereof. The present embodiments are therefore to be considered in all respects illustrative and not limiting, the scope of the invention being

indicated by the appended claims, and all modifications falling within the meaning and range of equivalency are intended to be embraced therein.

What is claimed is:

1. A frame-relay frame transmission circuit wherein, when a received frame-relay frame is written in a memory, said frame is written from an address shifted from the top of a frame buffer.

2. A frame-relay frame transmission circuit according to claim 1, wherein the shift size is determined for each connection.

3. A frame-relay frame transmission circuit for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising:

a processor for determining a shift size for each connection, said shift size by which said frame is to be shifted from the top address of a frame buffer;

a frame receiver for receiving said frame through said connection;

a memory for storing said received frame in a frame buffer from an address shifted from the top of a frame buffer by said shift size; and

a segmentation and reassembling device for reassembling said frame into said ATM cell.

4. A frame-relay frame transmission circuit according to claim 3, wherein said processor writes the set of a data link connection identifier (DLCI) and said shift size into a connection table, and retrieves said shift size in said connection table using said DLCI as a key.

5. A frame-relay frame transmission circuit according to claim 3, wherein said frame received by said frame receiver is transmitted to said memory through direct memory access.

6. A method for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising the steps of:

determining a shift size for each connection by which said frame is to be shifted from the top address of a frame buffer in a memory;

receiving said frame and writing said frame from an address shifted from the top address of said frame buffer by said shift size; and

reassembling said frame into an ATM cell.

7. A method according to claim 6, further comprising the steps of:

writing a set of a data link connection identifier (DLCI) and said shift size into a connection table; and

retrieving said shift size in said connection table using said DLCI as a key.

8. A method according to claim 6, wherein said received frame is transmitted to said memory through direct memory access.

9. A computer readable medium containing program instructions for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell, the program instructions including instructions for performing the steps comprising:

determining a shift size for each connection by which said frame is to be shifted

from the top address of a frame buffer in a memory;

receiving said frame and writing said frame from an address shifted from the top address of said frame buffer by said shift size; and

reassembling said frame into an ATM cell.

10. A computer readable medium according to claim 9, wherein said program instructions include instructions for:

writing a set of a data link connection identifier (DLCI) and said shift size into a connection table; and

retrieving said shift size in said connection table using said DLCI as a key.

11. A computer readable medium according to claim 9, wherein said received frame is transmitted to said memory through direct memory access.

ABSTRACT

The frame-relay frame transmission circuit of the present invention for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprises: a processor for determining a shift size for each connection, the shift size by which the frame is to be shifted from the top address of a frame buffer; a frame receiver for receiving the frame through the connection; a memory for storing the received frame in a frame buffer from an address shifted from the top of a frame buffer by the shift size; and a segmentation and reassembling device for reassembling the frame into the ATM cell.

FIG.1

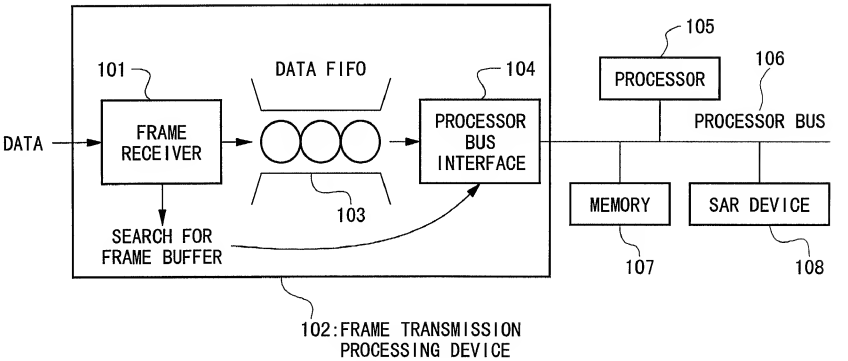


FIG.2

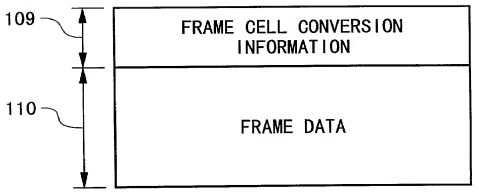

109
FRAME CELL CONVERSION INFORMATION
110
FRAME DATA

FIG.4

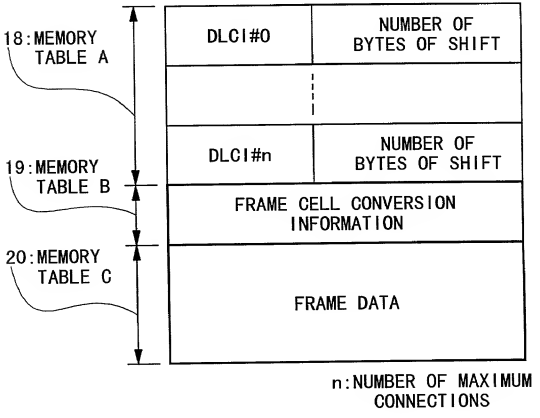

18:MEMORY TABLE A
DLCI#0
NUMBER OF BYTES OF SHIFT
DLCI#n
NUMBER OF BYTES OF SHIFT
19:MEMORY TABLE B
FRAME CELL CONVERSION INFORMATION
20:MEMORY TABLE C
FRAME DATA
n:NUMBER OF MAXIMUM CONNECTIONS

FIG.3

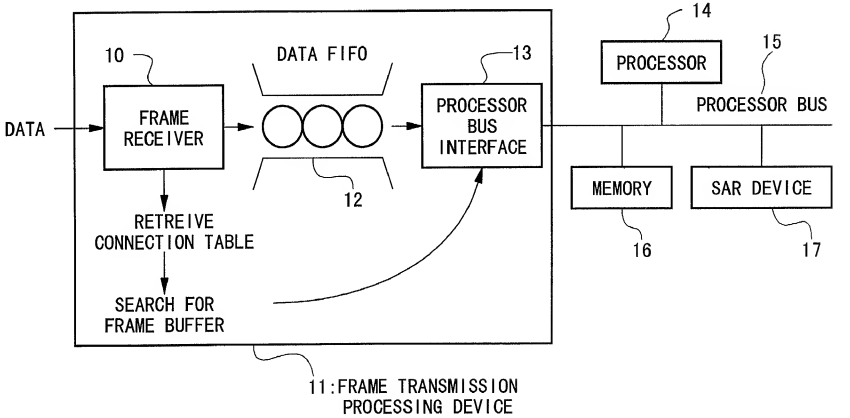
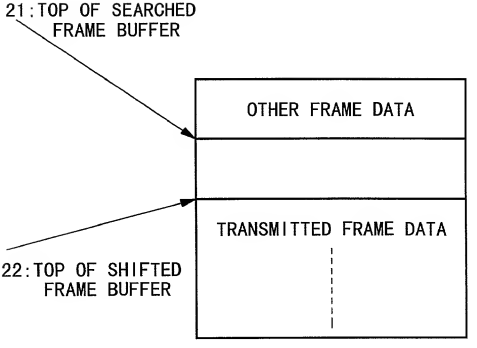

14
PROCESSOR
15
PROCESSOR BUS
10
DATA FIFO
13
DATA
FRAME RECEIVER
PROCESSOR BUS INTERFACE
MEMORY
SAR DEVICE
12
16
17
RETREIVE CONNECTION TABLE
SEARCH FOR FRAME BUFFER
11:FRAME TRANSMISSION PROCESSING DEVICE

FIG.5



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FRAME-RELAY FRAME TRANSMISSION CIRCUIT

the specification of which is attached hereto, unless the following box is checked:

☐ was filed on ______ as United States patent Application Number or PCT International patent application number ______ and was amended on ______ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Japan	Patent 9-359899	26/12/1997	YES X NO ___
			YES ___ NO ___
			YES ___ NO ___

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby appoint OSTROLENK, FABER, GERB & SOFFEN, and the members of the firm, Marvin C. Soffen - Reg. No. 17,542; Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,400; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William O. Gray, III - Reg. No. 30,944 and Louis C. Dujmich - Reg. No. 30,625, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

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RESIDENCE	COUNTRY OF CITIZENSHIP

POST OFFICE ADDRESS

FULL NAME OF THIRD JOINT INVENTOR (IF ANY)	INVENTOR'S SIGNATURE	DATE

RESIDENCE	COUNTRY OF CITIZENSHIP

POST OFFICE ADDRESS

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